How to adapt a board files-based project for ZedBoard Rev. E with 1GB RAM

1 Abstract

This document describes the procedure that updates a ZedBoard project based on board files to ZedBoard Rev. E loaded with 1GB of total DDR3 RAM.

2 Context

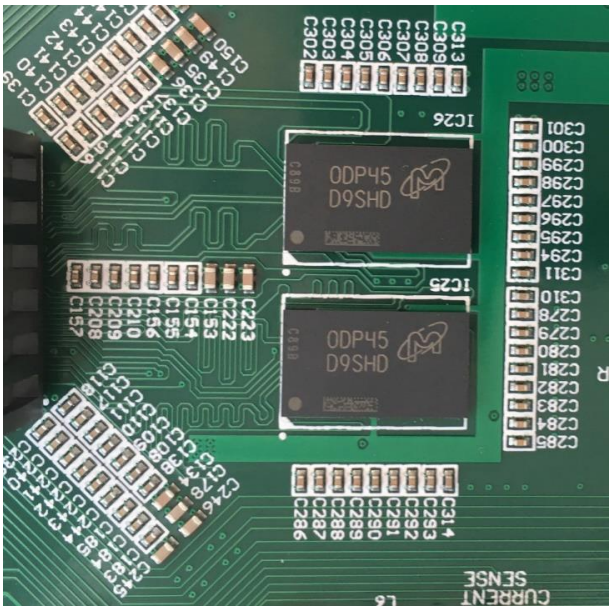
Some articles of revision E of ZedBoard development boards have 1GB total DDR3 memory. All the previous revisions have 512MB total DDR3 memory. The memory part change makes Rev. E incompatible with the already built projects for ZedBoard (e.g. demos, reference projects). Also, the projects that are designed using ZedBoard board file do not work properly due to DDR3 memory misconfiguration. However, one can solve this issue by changing the DDR3 memory part configuration and re-building the project, as described in this document.

2.1 Identifying affected boards

Only some articles of revision E of the ZedBoard are affected. These articles came loaded with 4Gb (32 Meg x 16 x 8) instead of 2Gb (16 Meg x 16 x 8) parts.

4Gb parts are identified by part number MT41x256M16, whereas 2Gb parts are identified by part number MT41x128M16.

To obtain the part number for the memory chip access https://www.micron.com/support/tools-and-utilities/fbga?fbga=D9SHD#pnlFBGA and introduce the FBGA Code (see Micron's instructions). The DDR memory is located on the left side of IC16 (Zynq chip). If the part number is MT41x256M16, you must update the project.



You only need to follow the instructions in this document if the memory parts on your ZedBoard are of 4Gb.

3 Requirements

- ZedBoard Rev. E with 1GB memory (MT41K**256**M16TW-107),
- Any hardware component required by the project that you want to update (e.g. pmods, fmc module),
- Vivado + SDK/Vitis (use the version that the original project was built in).

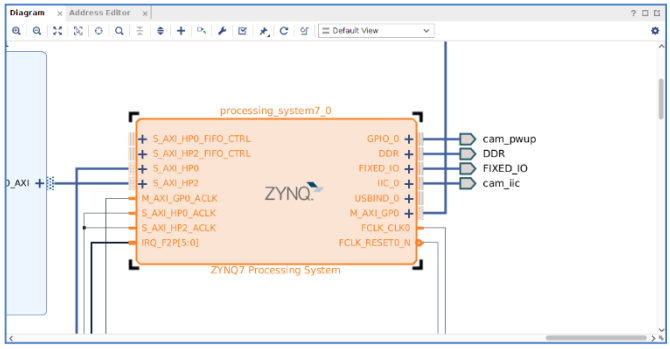
4 Update procedure

Step 1

Open the project in Vivado. Open Block Design.

Step 2

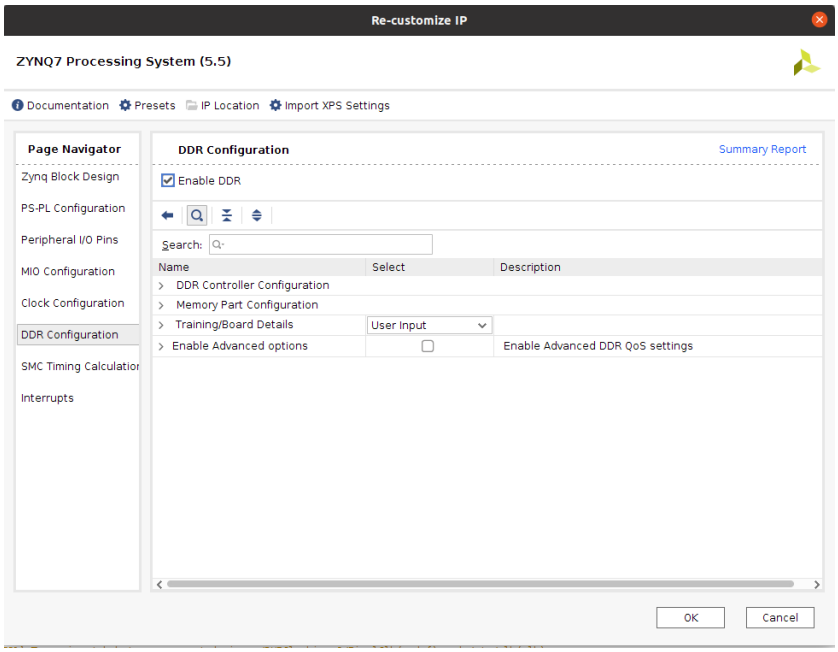
Find the Zynq IP in block diagram.



Step 3

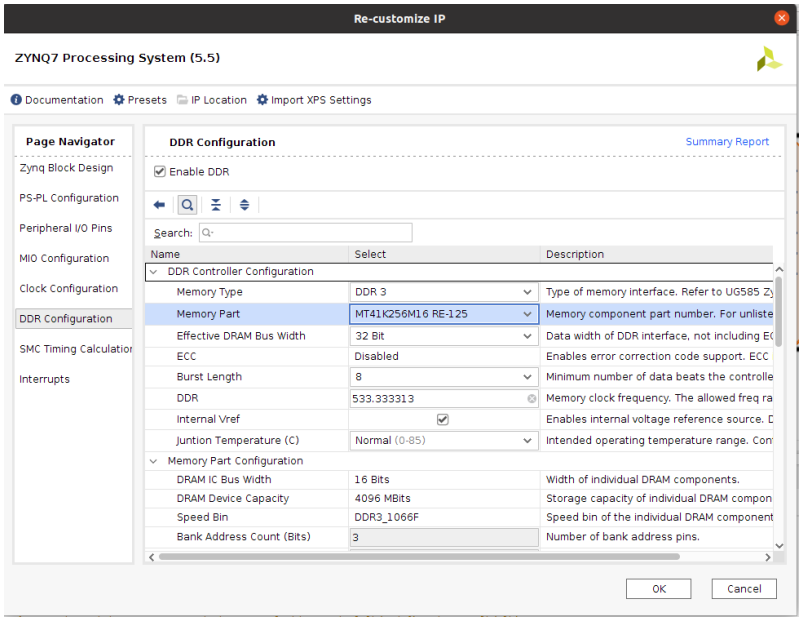
Open Zynq7 Processing System Re-customize IP by double clicking on Zynq IP.

Navigate to DDR Configuration from Page Navigator.



Step 4

Change the memory part to MT41K256M16 RE-125. Click OK.



Step 5

Validate design (F6). Save Block Design.

Step 6

Generate Bitstream.

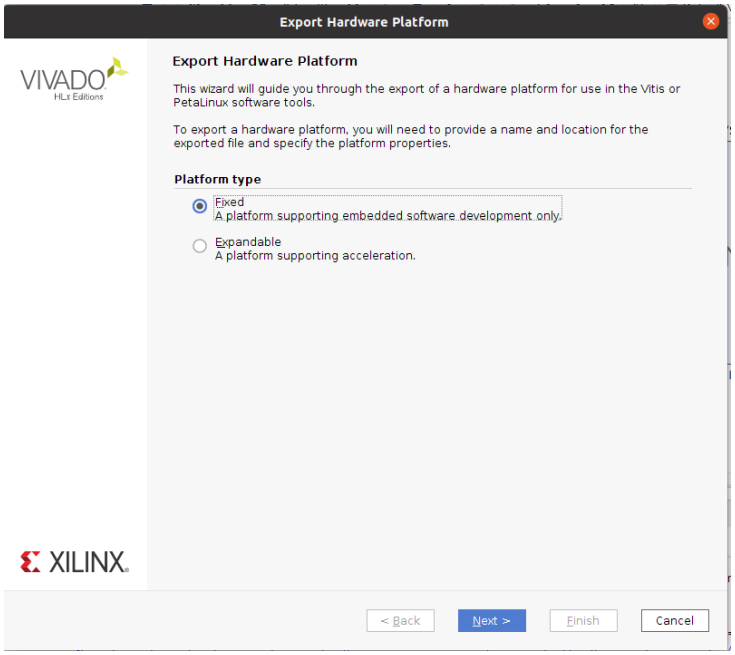
Step 7

After Bitstream generation completion export hardware. Click File → Export → Export Hardware.

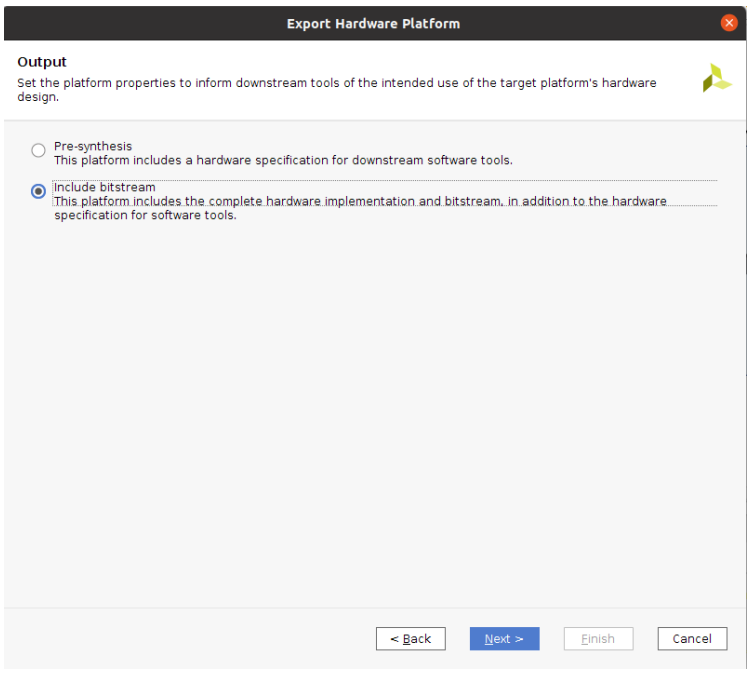
Vivado 2019.2 or greater

If you are using Vivado 2019.2 or greater:

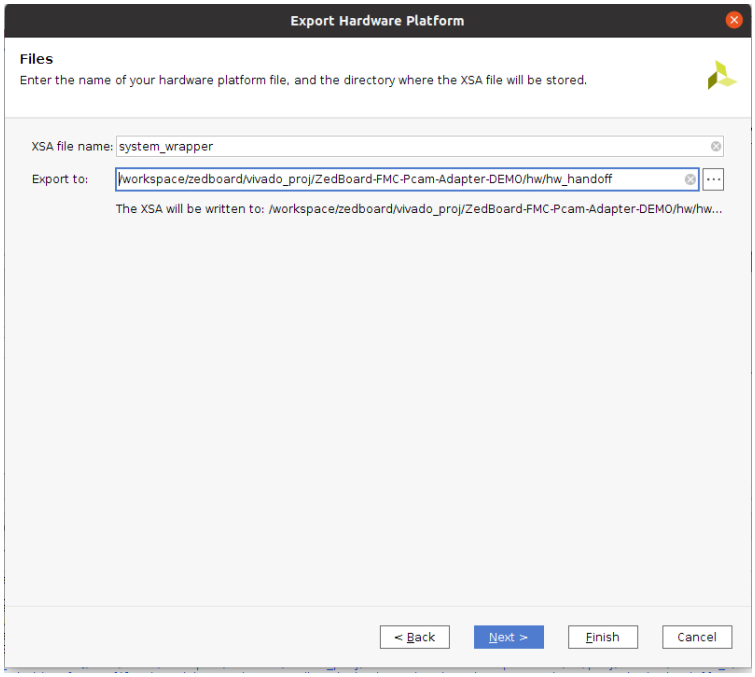
Use the Fixed option for Platform Type. Click Next.



Include Bitstream. Click Next.



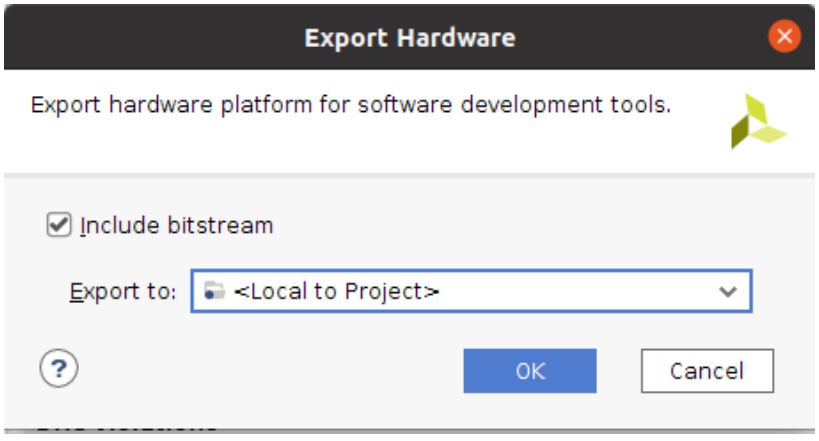
Save the hardware platform in a known folder. For most Digilent projects hw_handoff folder is used.



Vivado 2019.1 or lower

If you are using Vivado 2019.1 or lower:

Include Bitstream. Save the hardware platform in a known folder. For most Digilent projects hw_handoff folder is used.



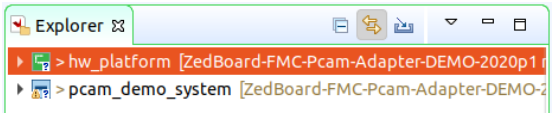
Step 8

Update the Hardware Platform from SDK/Vitis.

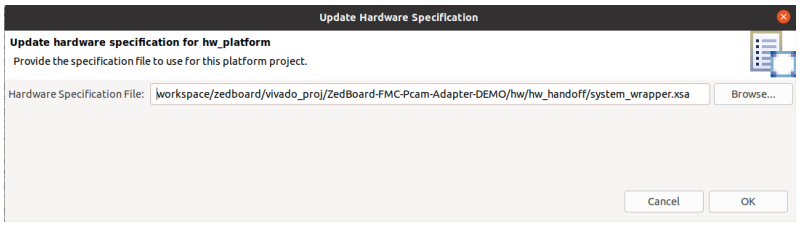
Vitis

If you are using Vitis:

Open the project in Vitis and Right Click on Platform Project → Update Hardware Specification



Enter the path to the exported hardware location.



Rebuild the Platform Project: Right Click on Platform Project → Build Project

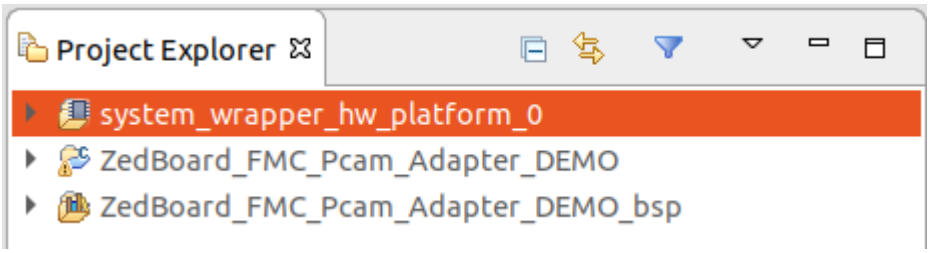
Rebuild the application: Right Click on application → Build Project

Now the project is ready to be uploaded on ZedBoard.

SDK

If you are using SDK:

Open the project in SDK.



Right Click on system wrapper hardware platform → Change Hardware Platform Specification → Click Yes in the Warning window → Enter the path to the exported hardware location → Click OK.

Rebuild the application: Right Click on application → Build Project

Now the project is ready to be downloaded to the ZedBoard.